# SRC Instructions: Increasing order of op-codes

| Description | | | | Mnemonic | 31 | 30 | 29 | 28 | 27 |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |
| | | | | | Opcode | | | | |
| **No operation** | | | | nop | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | |
| | | | | | Opcode | | | | |
| **Load register** | | | | ld | 0 | 0 | 0 | 0 | 1 |
| **Load relative register** | | | | ldr | 0 | 0 | 0 | 1 | 0 |
| **Store register** | | | | st | 0 | 0 | 0 | 1 | 1 |
| **Store relative register** | | | | str | 0 | 0 | 1 | 0 | 0 |
| **Load address** | | | | la | 0 | 0 | 1 | 0 | 1 |
| **Load relative address** | | | | lar | 0 | 0 | 1 | 1 | 0 |
| | | | | | | | | | |
| **Branch when ...** | Condition | | | | Opcode | | | | |
| never | 0 | 0 | 0 | brnv | 0 | 1 | 0 | 0 | 0 |
| always | 0 | 0 | 1 | br | 0 | 1 | 0 | 0 | 0 |
| zero | 0 | 1 | 0 | brzr | 0 | 1 | 0 | 0 | 0 |
| non zero | 0 | 1 | 1 | brnz | 0 | 1 | 0 | 0 | 0 |
| postive (including zero) | 1 | 0 | 0 | brpl | 0 | 1 | 0 | 0 | 0 |
| negative | 1 | 0 | 1 | brmi | 0 | 1 | 0 | 0 | 0 |
| **Branch and link when ...** | | | | | | | | | |
| never | 0 | 0 | 0 | brlnv | 0 | 1 | 0 | 0 | 1 |
| always | 0 | 0 | 1 | brl | 0 | 1 | 0 | 0 | 1 |
| zero | 0 | 1 | 0 | brlzr | 0 | 1 | 0 | 0 | 1 |
| non zero | 0 | 1 | 1 | brlnz | 0 | 1 | 0 | 0 | 1 |
| postive (including zero) | 1 | 0 | 0 | brlpl | 0 | 1 | 0 | 0 | 1 |
| negative | 1 | 0 | 1 | brlmi | 0 | 1 | 0 | 0 | 1 |

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| | | Opcode | | | | |
|---|---|---|---|---|---|---|
| **2's complement addition** | add | 0 | 1 | 1 | 0 | 0 |
| **Immediate 2's complement addn.** | addi | 0 | 1 | 1 | 0 | 1 |
| **2's complement subtraction** | sub | 0 | 1 | 1 | 1 | 0 |
| **Negate** | neg | 0 | 1 | 1 | 1 | 1 |
| **Logical And** | and | 1 | 0 | 1 | 0 | 0 |
| **Immediate logical And** | andi | 1 | 0 | 1 | 0 | 1 |
| **Logical Or** | or | 1 | 0 | 1 | 1 | 0 |
| **Immediate logical Or** | ori | 1 | 0 | 1 | 1 | 1 |
| **Not** | not | 1 | 1 | 0 | 0 | 0 |
| | | | | | | |
| | | Opcode | | | | |
| **Shift right by count** | shr | 1 | 1 | 0 | 1 | 0 |
| **Shift right by count in a register** | shr | 1 | 1 | 0 | 1 | 0 |
| **AShift right by count** | shra | 1 | 1 | 0 | 1 | 1 |
| **AShift right by count in a register** | shra | 1 | 1 | 0 | 1 | 1 |
| **Shift left by count** | shl | 1 | 1 | 1 | 0 | 0 |
| **Shift left by count in a register** | shl | 1 | 1 | 1 | 0 | 0 |
| **Shift circ. by count** | shc | 1 | 1 | 1 | 0 | 1 |
| **Shift circ. by count in a register** | shc | 1 | 1 | 1 | 0 | 1 |
| | | | | | | |
| | | opcode | | | | |
| **Halt machine** | stop | 1 | 1 | 1 | 1 | 1 |