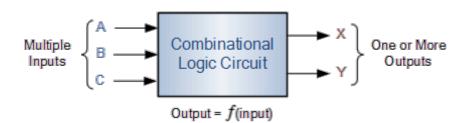
Lab Experiment # 09 <u>Building logic circuits using Multiplexers</u>

Objectives

• To learn how to build combinational logic circuits using multiplexers.

Background

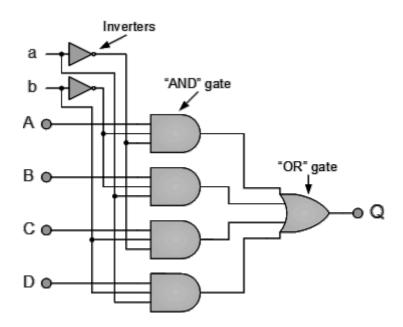
In a **Combinational Logic Circuit**, the output is dependent at all times on the combination of its inputs. Some examples of a combinational circuit include **Multiplexers**, **De-multiplexers**, **Encoders**, **Decoders**, **Full** and **Half Adders** etc.



A Multiplexer is a combination of logic gates resulting into circuits with two or more inputs (data inputs) and one output.

4 Channel Multiplexer using Logic Gates

The following circuit shows a 4x1 mux. Based on the binary value placed at the inputs "a" and "b", what will appear at the circuit output Q is one of the following values: A, B, C, or D.



The circuit above is implemented based on the following truth table.

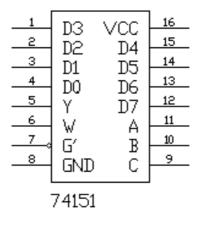
a	b	Q
0	0	А
0	1	В
1	0	С
1	1	D

Drawing Multiplexers in EWB:

Task: Draw the previous lab examples using EWB, follow the steps below to implement Multiplexers and Decoders.

0 😨 📮 🗘 🕅 🖻		
Digital 唐王 唐王 惠 報報 報報 MUX DEC ENC +-×+ 123		
2 MUX	Generic 1-of-8 MUX 74139 (Dual 2-to-4 Dec/DEMUX) 74150 (1-of-16 Data Sel/MUX) 74151 (1-of-8 Data Sel/MUX) 74153 (Dual 4-to-1 Data Sel/MUX) 74157 (Duad 2-to-1 Data Sel/MUX)	

Then choose 74151 (1-of-8 Data Sel/MUX) from the list:



You may also choose 74150 (1-of-16 Data Sel/Mux) as follows

1 3 4 5 6 7 8 9	E7 E6 E5 E4 E3 E2 E1 E0 G' ¥	VCC E8 E10 E11 E12 E13 E14 E15 A	24 23 22 21 20 19 18 18 17 16 15
10 11 12	G' W D GND	E15 A B C	
	74150		

NOTE: the "A" line in the multiplexer is the least significant bit, while "C" is the most significant bit.

Data selector/multiplexer truth table:

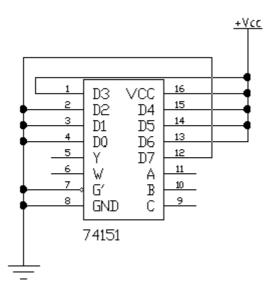
Sel	Select		Strobe	Outp	outs
С	B	Α	G'	W	Y
х	Х	Х	1	1	0
0	0	0	0	D0'	D0
0	0	1	0	D1'	D1
0	1	0	0	D2'	D2
0	1	1	0	D3'	D3
1	0	0	0	D4'	D4
1	0	1	0	D5'	D5
1	1	0	0	D6'	D6
1	1	1	0	D7'	D7

Multiplexers can be used to synthesize logic functions

4-to-1 MUX can realize any 3-variable function, 8-to-1 MUX can realize a 3-variable or 4-variable function, in general 2^{n} -to-1 MUX can realize an (n+1)-variable and n-variable function.

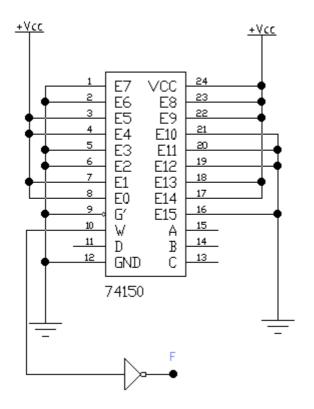
Example: realizing functions using Multiplexers

The function F=A'BC+AB'+AC' Can be implemented using an 8-1 mux as follows



Example: realizing functions using Multiplexers

The function F= A'C'+B'C'+C'D+ABCD' Can be implemented using an 16-1 mux as follows



Example: realizing a 4-variable function using 8-to-1Multiplexer

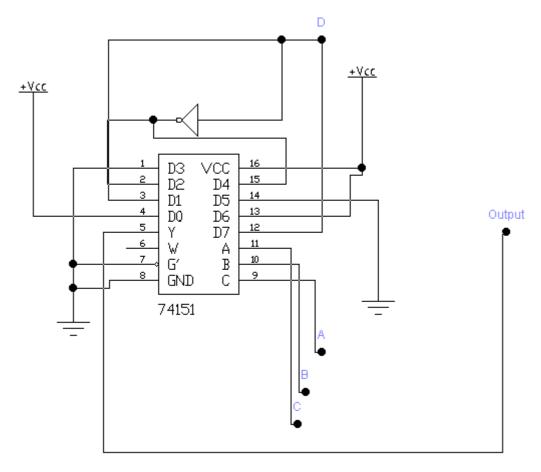
F(A, B, C, D) = A'B'C'D' + A'B'C'D + A'B'CD + A'BC'D' + ABC'D' + ABC'D' + ABC'D + ABCD

Truth table:

	Α	B	С	D	F	
0	0	0	0	0	1	E -1
1	0	0	0	1	1	Г-1

2	0	0	1	0	0	F=D
3	0	0	1	1	1	г–р
4	0	1	0	0	1	F=D'
5	0	1	0	1	0	г–D
6	0	1	1	0	0	F=0
7	0	1	1	1	0	г-0
8	1	0	0	0	1	F=D'
9	1	0	0	1	0	г–D
10	1	0	1	0	0	F=0
11	1	0	1	1	0	г-0
12	1	1	0	0	1	F=1
13	1	1	0	1	1	г-1
14	1	1	1	0	0	F=D
15	1	1	1	1	1	г–D

To implement this function using EWB, you draw the following circuit:



<u>Lab Tasks</u>

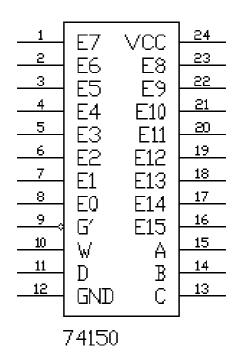
Task 1: Implementing single-output circuits using muxes

Implement the following function using one 8x1 multiplexer F(A, B, C, D) = A'B'C'D'+A'B'C'D+A'B'CD+A'BC'D'+ABC'D'+ABC'D'+ABC'D+ABCD

Note: this example has already been solved above. Just draw the circuit using EWB.

Task 2: Implementing single-output circuits using muxes

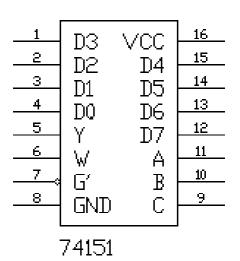
Implement the following function using one 16x1 multiplexer F(A, B, C, D) = A'C'B+AB'C'+B'C'D+ABCD'



Task 3: Implementing single-output circuits using muxes

Implement the following function using one 8x1 multiplexer F(A, B, C, D) = A'C'B+AB'C'+B'C'D+ABCD'

	Α	В	С	D	F	
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
10	1	0	1	0		
11	1	0	1	1		
12	1	1	0	0		
13	1	1	0	1		
14	1	1	1	0		
15	1	1	1	1		



Task 4: Problems with verbal description

Design a combinational circuit (using two 8-to-1 multiplexers) with three inputs, and one output to implement the following function.

	Α	В	С	D	F
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	0
12	1	1	0	0	1
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	1

1 2 3 4 5 6 7 8	D3 D2 D1 D0 Y G' GND	VCC D4 D5 D6 D7 A B C	16 15 14 13 12 11 10 9
	GND	U	

$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	D2 D1 D0 Y W G'	D4 <u>15</u> D5 <u>14</u> D5 <u>13</u> D6 <u>13</u> D7 <u>12</u> A <u>11</u>
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