Lab Experiment # 13

Design and Implementation of Magnitude Comparator

Objective

To design and implement

(i) 2 – Bit magnitude comparator using basic gates.

(ii) 8 – Bit magnitude comparator using IC 7485.

Parts Required

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	AND GATE	IC 7408	2
2.	X-OR GATE	IC 7486	1
3.	OR GATE	IC 7432	1
4.	NOT GATE	IC 7404	1
5.	4-BIT MAGNITUDE COMPARATOR	IC 7485	2

Theory:

The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is combinational circuits that compares two numbers A and B and determine their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B or A<B.

A = A3 A2 A1 A0 B = B3 B2 B1 B0

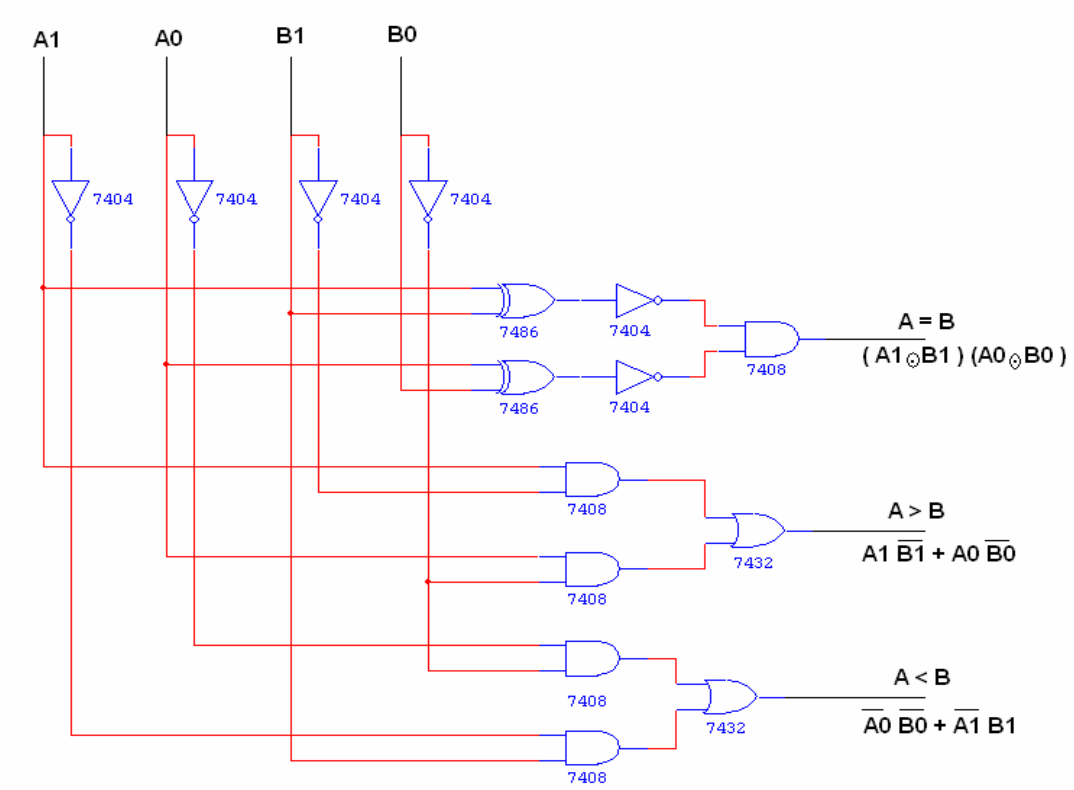
The equality of the two numbers and B is displayed in a combinational circuit designated by the symbol (A=B).

This indicates A greater than B, then inspect the relative magnitude of pairs of significant digits starting from most significant position. A is 0 and that of B is 0.

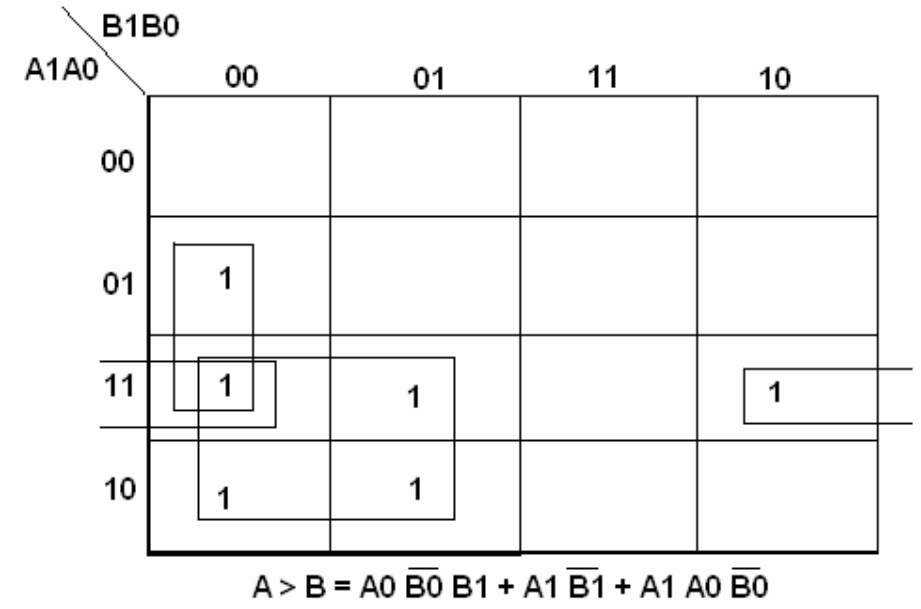
We have A<B, the sequential comparison can be expanded as

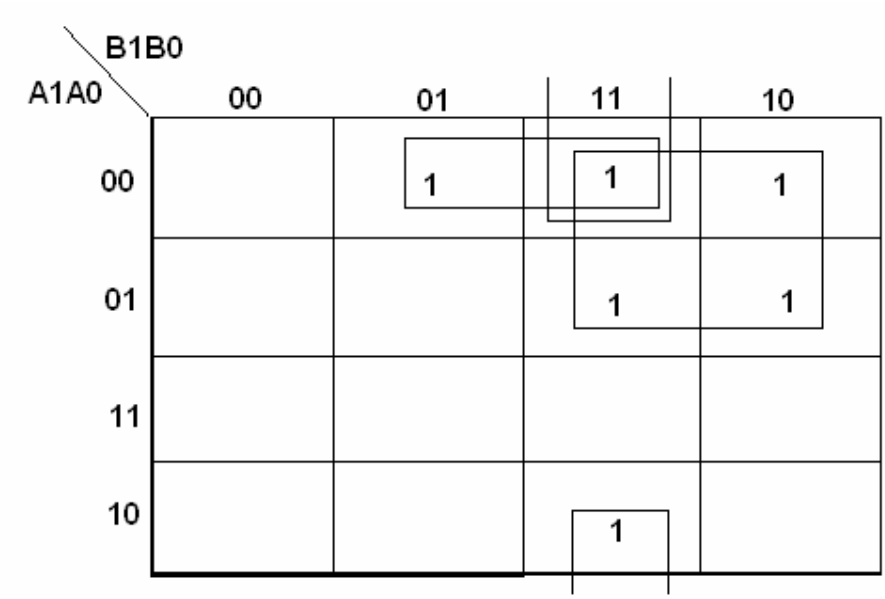
A>B = A3B31 + X3A2B2 + X3X2A1B1 + X3X2X1A0B0 A_1<B = A31B3 + X3$A_1$21B2 + X3X2A11B1 + X3X2X1A01B0

Logic Diagram:
2 Bit Magnitude Comparator

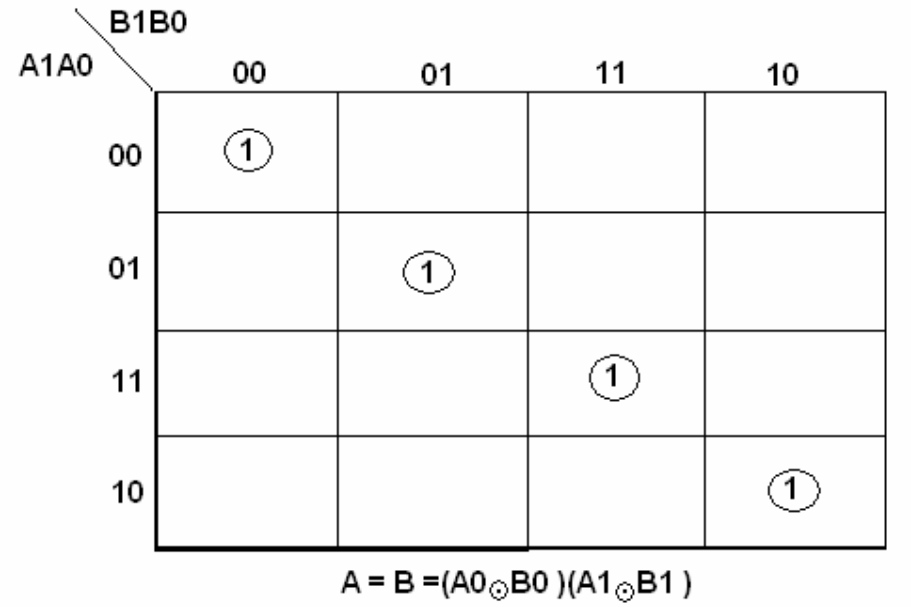


K MAP


B1B0
A1A0
00
01
11
10
00
01
11
10
1
1
1
1
1
1
A > B = A0 $\overline{B0}$ B1 + A1 $\overline{B1}$ + A1 A0 $\overline{B0}$



$A < B = \overline{A1}\ \overline{A0}\ B0 + \overline{A0}\ B0\ B1 + \overline{A1}\ B1$

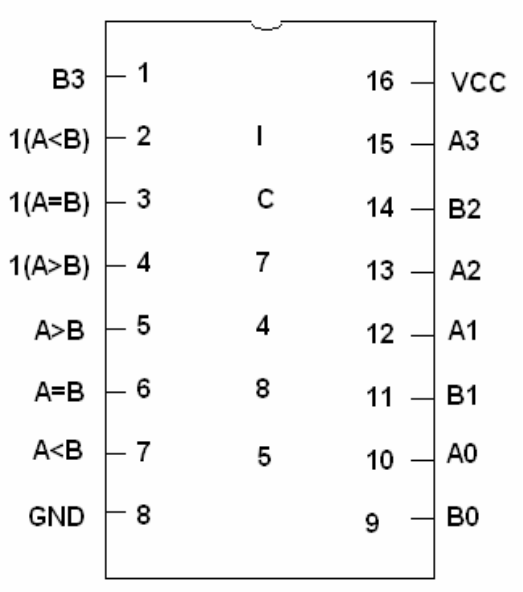


$A = B = (A0 \odot B0)(A1 \odot B1)$

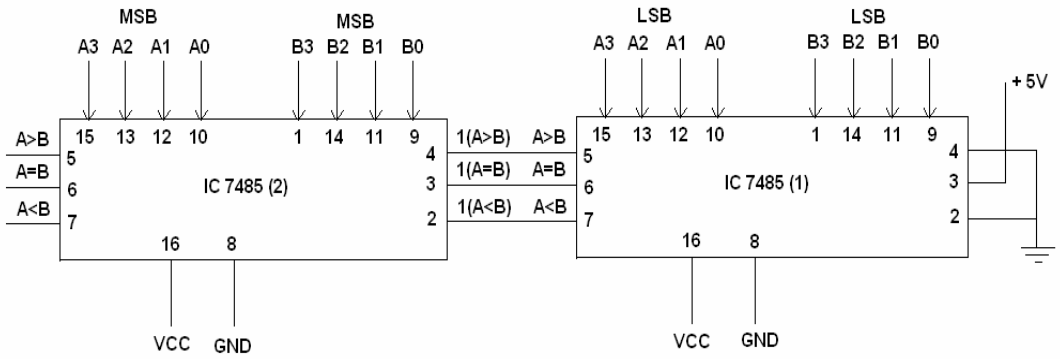
Truth Table

A	A	B	B	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Pin Diagram For IC 7485



Logic Diagram
8 Bit Magnitude Comparator



Truth Table

A	B	A>B	A=B	A<B
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	1	0
0 0 0 1 0 0 0 1	0 0 0 0 0 0 0 0	1	0	0
0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 1	0	0	1

Procedure

(i) Verify the gates
(ii) Connections are given as per circuit diagram.
(iii) Logical inputs are given as per circuit diagram.
(iv) Observe the output and verify the truth table.