

## Lab Experiment # 12

### Design and Implementation of Code Convertor

#### Objective

To design and implement 4-bit

- (i) Binary to gray code converter
- (ii) Gray to binary code converter
- (iii) BCD to excess-3 code converter
- (iv) Excess-3 to BCD code converter

#### Parts required:-

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	X-OR GATE	IC 7486	1
2.	AND GATE	IC 7408	1
3.	OR GATE	IC 7432	1
4.	NOT GATE	IC 7404	1

#### Equipment required:-

- Trainer/ proto board
- Wire cutter
- Patch Cords
- Voltmeter

#### Theory:

The availability of large variety of codes for the same discrete elements of information results in the use of different codes by different systems. A conversion circuit must be inserted between the two systems if each uses different codes for same information. Thus, code converter is a circuit that makes the two systems compatible even though each uses different binary code.

The bit combination assigned to binary code to gray code. Since each code uses four bits to represent a decimal digit. There are four inputs and four outputs. Gray code is a non-weighted code.

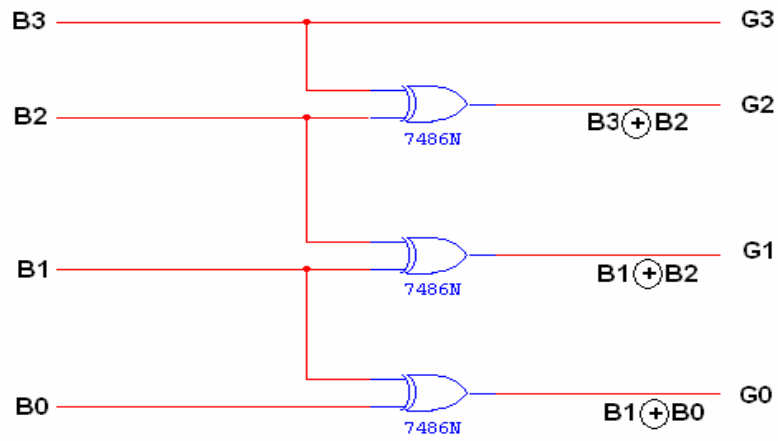
The input variable are designated as B3, B2, B1, B0 and the output variables are designated as C3, C2, C1, C0. from the truth table, combinational circuit is designed. The Boolean functions are obtained from K-Map for each output variable.

A code converter is a circuit that makes the two systems compatible even though each uses a different binary code. To convert from binary code to Excess-3 code, the input lines must supply the bit combination of elements as specified by code and the output lines generate the corresponding bit combination of code. Each one of the four maps represents one of the four outputs of the circuit as a

function of the four input variables.

A two-level logic diagram may be obtained directly from the Boolean expressions derived by the maps. These are various other possibilities for a logic diagram that implements this circuit. Now the OR gate whose output is  $C+D$  has been used to implement partially each of three outputs.

## Logic Diagram: Binary To Gray Code Convertor



K-Map for G<sub>3</sub>:

		B1B0			
		00	01	11	10
B3B2	00				
	01				
	11	1	1	1	1
	10	1	1	1	1

$$G_3 = B_3$$

K-Map for G<sub>2</sub>:

		B1B0			
		00	01	11	10
B3B2	00				
	01	1	1	1	1
	11				
	10	1	1	1	1

$$G2 = B3 \oplus B2$$

K-Map for  $G_1$ :

		B1B0			
		00	01	11	10
B3B2	00			1	1
	01	1	1		
	11	1	1		
	10			1	1

$G_1 = B_1 \oplus B_2$

K-Map for  $G_0$ :

		B1B0			
		00	01	11	10
B3B2	00		1		1
	01		1		1
	11		1		1
	10		1		1

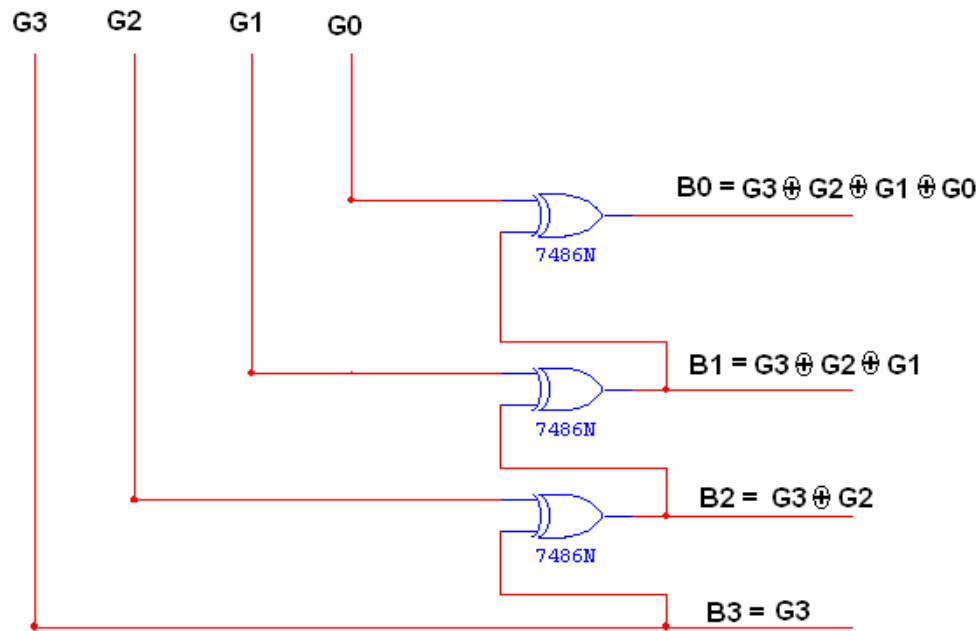
$G_0 = B_1 \oplus B_0$

**Truth Table:**

Binary input				Gray code output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

**Logic Diagram:**

**Gray Code To Binary Convertor**



K-Map for B<sub>3</sub>:

G3G2 \ G1G0		00	01	11	10
		00	01	11	10
00		0	0	0	0
01		0	0	0	0
11		1	1	1	1
10		1	1	1	1

B<sub>3</sub> = G<sub>3</sub>

K-Map for B<sub>2</sub>:

G3G2 \ G1G0		00	01	11	10
		00	01	11	10
00		0	0	0	0
01		1	1	1	1
11		0	0	0	0
10		1	1	1	1

$$B_2 = G_3 \oplus G_2$$

K-Map for B<sub>1</sub>:

		G1G0			
		00	01	11	10
G3G2	00	0	0	1	1
	01	1	1	0	0
	11	0	0	1	1
	10	1	1	0	0

K-Map for B<sub>0</sub>:

$$B_1 = G_3 \oplus G_2 \oplus G_1$$

		G1G0			
		00	01	11	10
G3G2	00	0	①	0	①
	01	①	0	①	0
	11	0	①	0	①
	10	①	0	①	0

$$B_0 = G_3 \oplus G_2 \oplus G_1 \oplus G_0$$

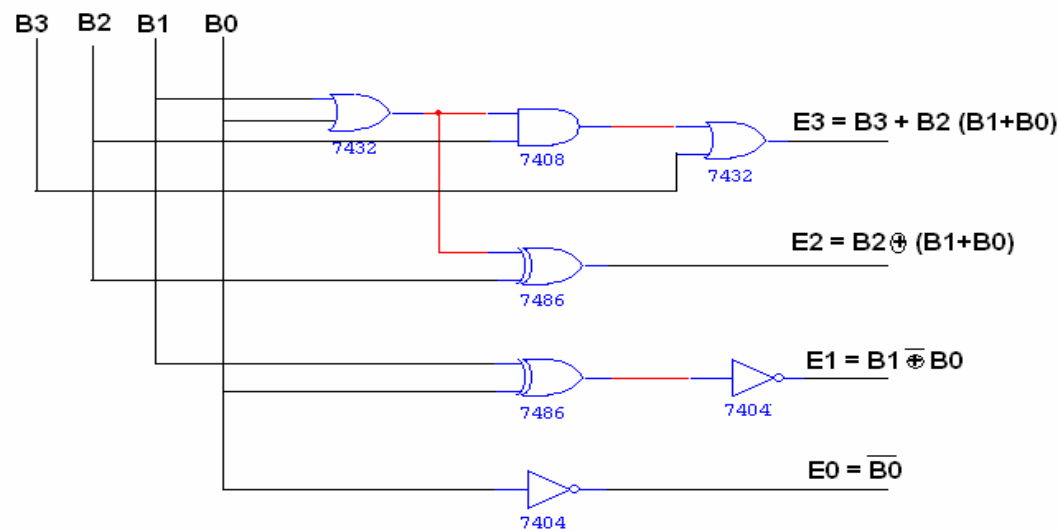


**Truth Table:**

Gray Code				Binary Code			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

**Logic Diagram:**

**Bcd To Excess-3 Convertor**



K-Map for E3:

		B1B0			
		00	01	11	10
B3B2	00				
	01		1	1	1
	11	x	x	x	x
	10	1	1	x	x

$E3 = B3 + B2(B0 + B1)$

		B1B0			
		00	01	11	10
B3B2	00		1	1	1
	01	1			
	11	x	x	x	x
	10		1	x	x

$$E2 = B2 \oplus (B1 + B0)$$

K-Map for E2:

K-Map for E<sub>1</sub>:

		B1B0			
		00	01	11	10
B3B2	00	1		1	
	01	1		1	
	11	x	x	x	x
	10	1		x	x

$$E_1 = B_1 \oplus B_0$$

K-Map for E<sub>0</sub>:

		B1B0			
		00	01	11	10
B3B2	00	1			1
	01	1			1
	11	x	x	x	x
	10	1		x	x

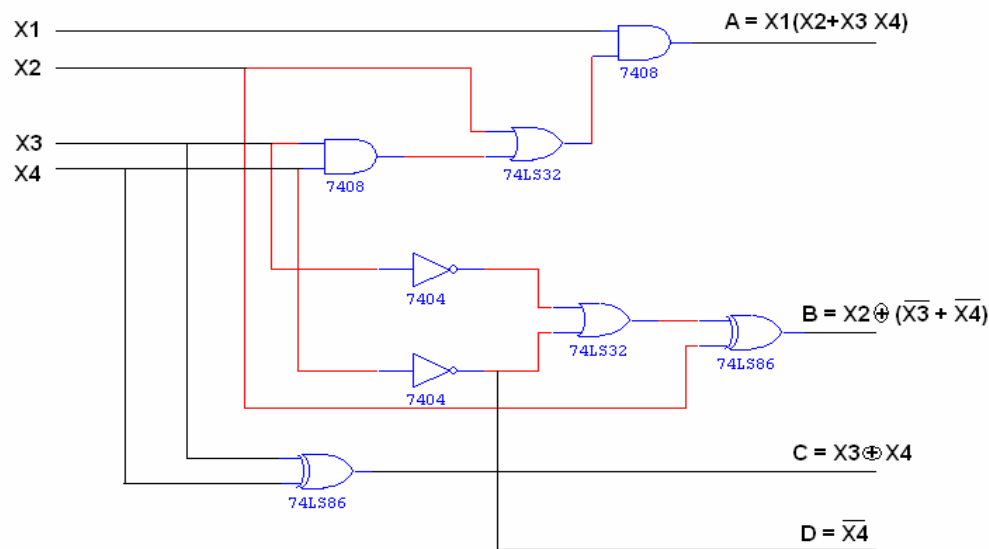
$$E_0 = \overline{B_0}$$

**Truth Table:**

BCD input				Excess – 3 output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

**Logic Diagram:**

**Excess-3 To Bcd Convertor**



K-Map for A:

X1 X2 \ X3 X4					
		00	01	11	10
X1 X2	00	X	X	0	X
	01	0	0	0	0
	11	1	X	X	X
	10	0	0	1	0

$$A = X1 X2 + X3 X4 X$$

K-Map for B:

X1 X2 \ X3 X4					
		00	01	11	10
00	X	X	0	X	
01	0	0	1	0	
11	0	X	X	X	
10	1	1	0	1	

$$B = X2 \oplus (\overline{X3} + \overline{X4})$$

K-Map for C:

X3 X4 X1 X2					
		00	01	11	10
00	X	X	0	X	
01	0	1	X	1	
11	0	X	X	X	
10	X	1	0	1	

$$C = X3 \oplus X4$$

K-Map for D:

X1 X2 \ X3 X4					
		00	01	11	10
00	X	X	0	X	
01	1	0	0	1	
11	1	X	X	X	
10	1	0	0	1	

$$D = \overline{X4}$$

**Truth Table:**

Excess – 3 Input				BCD Output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

**Procedure:**

- (i) verify the gates
- (ii) Connect the proper power supply
- (iii) Connections were given as per circuit diagram.
- (iv) Logical inputs were given as per truth table
- (v) Observe the logical output and verify with the truth tables.